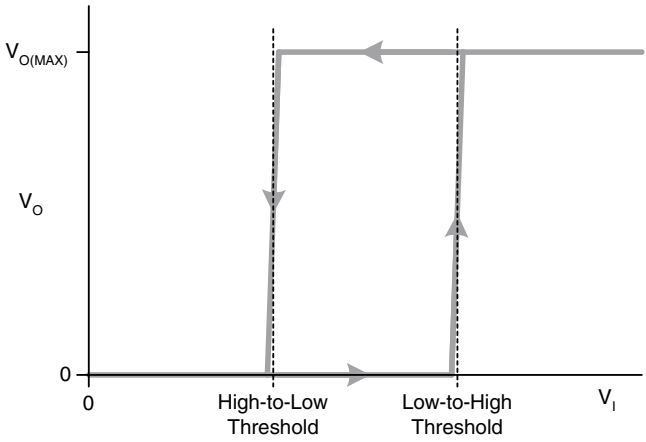

FIGURE 14.31 Hysteresis loop.

The degree of hysteresis designed into a comparator circuit is determined by the difference between the high and low thresholds. A small difference is less tolerant of noise. However, a larger difference has a more muted response, which must be considered in its effects on a system's behavior. Dual comparison thresholds that create hysteresis are implemented by applying positive feedback rather than negative feedback to an op-amp or comparator. Such a circuit is shown in Fig. 14.32. The circuit looks very similar to a conventional closed-loop amplifier, but the feedback is applied to the positive terminal rather than the negative terminal.

The positive feedback through R2 results in a voltage at the positive terminal that is determined by the basic voltage divider expression,

$$v_+ = v_O + (v_I - v_O)\frac{R2}{R1+R2} = v_O\left(1 - \frac{R2}{R1+R2}\right) + v_I\frac{R2}{R1+R2} = v_O\frac{R1}{R1+R2} + v_I\frac{R2}{R1+R2}$$

Therefore, the output pulls v_+ down when it is low and pulls v_+ up when it is high. This means that, if v_I is increasing and trying to switch the comparator state from low to high, it must be raised to a higher voltage threshold to counteract the pull-down effect when the comparator's output is al-

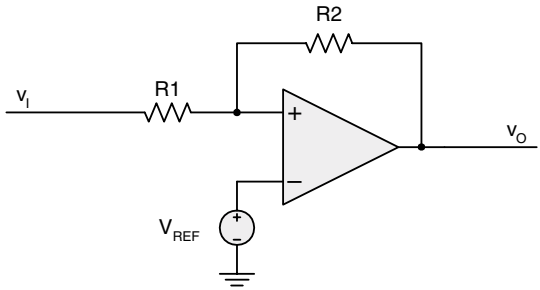

FIGURE 14.32 Hysteresis created by positive feedback.

ready low. Similarly, v_I must be reduced to a lower voltage threshold to counteract the pull-up effect when the output is already high.

Another benefit of hysteresis is that it "snaps" the comparator input voltage above or below V_{REF} once the output state transition is triggered. This forces what might otherwise be a gradually rising input signal into a sharp edge that improves the switching time of the comparator's output. Any time spent in a region of linear amplification as a result of $v_I \approx V_{REF}$ is minimized in favor of a rapid transition to saturation in either the high or low output state.

The voltage at the positive terminal must be brought to V_{REF} to cause a comparator state change. Therefore, the general relationships for the low-to-high and high-to-low thresholds, V_{TLH} and V_{THL}, can be written by substituting V_{REF} for v_+ and the appropriate threshold for v_I.

$$V_{TLH} = V_{REF}\frac{R1+R2}{R2} - V_{OL}\frac{R1}{R2} \text{ and } V_{THL} = V_{REF}\frac{R1+R2}{R2} - V_{OH}\frac{R1}{R2}$$

These relationships assume an ideal comparator that has zero input bias current. Real-world effects of I_{BIAS} can be reduced by using resistors that are not too large. If hundreds of microamps or a milliamp are designed to flow through the R1/R2 resistor network, the nanoamps of input bias current will likely introduce negligible error into the system.

To illustrate the application of hysteresis in a real circuit, consider a common bipolar comparator, the LM311, connected such that it drives an approximate output range of 0 V (V_{OL}) to 5 V (V_{OH}). It is desired to convert an incoming analog signal ranging from 0 to 3 V into a digital output. The halfway threshold of 1.5 V is chosen to differentiate between logical 1 and 0. However, it is known that the input signal can have noise of up to 500 mV peak-to-peak (p-p) superimposed on it. This means that a signal that is just over 1.5 V at one moment in time can abruptly drop to near 1 V a short while later. We do not want the LM311's output to swing every time a 500-mV noise spike happens to coincide with the rising and falling of the 3-V input signal. Therefore, at least 500 mV of hysteresis should be designed into the circuit.

It is decided to design in 600 mV of hysteresis for some added margin. Rather than establishing a single 1.5-V threshold for low-to-high and high-to-low triggering, two thresholds of 1.5 + 0.3 V and 1.5 – 0.3 V are desired, which combine to provide 600 mV of hysteresis. This configuration requires the input to rise above 1.8 V to be recognized as a logic 1 and requires the input to fall below 1.2 V to be recognized as a logic 0. Even if 500 mV of noise hits the input just after it reaches 1.8 V, the resulting 1.3 V level will be too high to trigger a return to logic 0.

The first design task is to calculate the ratio between the input and feedback resistors, R1 and R2. Recall that hysteresis is the difference between V_{TLH} and V_{THL}. The previously derived expressions for V_{THL} and V_{THL} can be simplified for this circuit, because V_{OH} and V_{OL} are already known.

$$V_{TLH} = V_{REF}\frac{R1+R2}{R2} \text{ and } V_{THL} = V_{REF}\frac{R1+R2}{R2} - 5\frac{R1}{R2}$$

Subtracting the two thresholds yields a relationship that can be used to solve for R1 and R2.

$$V_{TLH} - V_{THL} = V_{REF}\frac{R1+R2}{R2} - V_{REF}\frac{R1+R2}{R2} + 5\frac{R1}{R2} = 5\frac{R1}{R2} = 0.6 \text{ V}$$

It follows that R1 = 0.12R2. Because it is the ratio between R1 and R2 that is important rather than their actual values, these numbers can be multiplied by 10,000 to yield R1 = 1.2 kΩ and R2 = 10 kΩ, which are standard 5 percent tolerance resistance values. If more accurate 1 percent resistors are desired, R1 would be chosen as 1.21 kΩ, which is the closest 1 percent standard value.